

<b>Notice of References Cited</b>	Application/Control No. 10/624,614		Applicant(s)/Patent Under Reexamination LU, ZIYANG	
	Examiner Patrick J. Assouad		Art Unit 2857	Page 1 of 1

#### U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,715,093	03-2004	Farmer et al.	713/400
	B	US-2004/0158760 a1	08-2004	Farmer et al.	713/500
	C	US-6,557,128	04-2003	Turnquist, James Alan	714/724
	D	US-6,651,205	11-2003	Takahashi, Koji	714/738
	E	US-6,678,643	01-2004	Turnquist et al.	703/14
	F	US-2002/0184560 a1	12-2002	Wang et al.	714/25
	G	US-5,867,695	02-1999	Amini et al.	713/503
	H	US-6,557,133	04-2003	Gomes, Glen A.	714/738
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

#### FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

#### NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Sehgal et al., "SOC Test Planning Using Virtual Test Access Architectures", IEEE, 2004.			
	V	Schmid et al., "Advanced Synchronous Scan Test Methodology for Multi Clock Domain ASICs", IEEE, unknown date.			
	W	Ashkinazy et al., "Tools for Validating Asynchronous Digital Circuits", IEEE, 1994.			
	X				

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.